REMARKS

Claims 2-3, 6-13 and 16-21 are pending in the present application.

Claims 2-3, 12-13 and 20 were amended herein.

Reconsideration of the claims is respectfully requested.

35 U.S.C. § 112, First Paragraph (Written Description)

Claims 2-3, 6-13 and 16-19 were rejected under 35 U.S.C. § 112, first paragraph as failing to comply with the written description requirement. This rejection is respectfully traversed.

The Office Action states that the limitations "detection based upon the base and offset address values" and "without using a memory address corresponding to the first base and offset address values" appear to be new matter which were not described in the application in such a way as to reasonably convey to one skilled in the art that the inventors, at the time the application was filed, had possession of the claims invention.

However, the specification as filed teaches use of instruction that reference memory locations having an address computed by adding a base address value and an offset value:

> For example, an instruction that loads data from external memory has a format that refers to the specific location in external memory from which to load the data. The format can include a base address value and an offset address value, which are to be added to compute the effective reference address of the instruction 151. The base address value can be a constant value or specify a value found in an internal register of the microprocessor 100. Similarly, the offset address value can be a constant value or specify a value found in an internal register of the microprocessor.
>
> Similarly, an instruction that stores data to external memory has a format that refers to the specific location in external memory from which to store the data. The format can similarly include a base address value and an offset address value, which are used to compute the effective reference address of the instruction 151.
>
> The instruction decode stage 120 couples the parts of the instruction 151, including information about the base address value and the offset address value, to the address computation stage 130.

> The address computation stage 130 receives the base address value and the offset address value, and computes the effective reference address of the instruction 151.

Specification, page 7, line 15 to page 8, line 11. The specification then describes symbolic load-store bypass element 121 determining whether two instructions refer to an identical memory location from the base and offset values, by determining that the base value A and the offset value B of one instruction are identical to the base value A and the offset value B of another instruction, without computing the actual address referenced (i.e., without adding the base value A and offset value B for both instructions):

> The instruction decode stage 120 includes a symbolic load-store bypass element 121. The bypass element 121 examines the parts of the instruction 151, including information about what operations the instructions 151 command the microprocessor 100 to perform. If these operations are to load data from external memory, or to store data to external memory, the bypass element 121 further examines the syntax of any addresses 151 refer to as operands.
>
> If the operand addresses the instructions 151 refer to include identical base address values and offset address values, the bypass element 121 generates a bypass signal indicating that the instructions 151 refer to the same location in external memory.
>
> *When the bypass signal is generating, the address computation stage 130, does not have to compute the actual effective address for the microprocessor 100 to act on the knowledge that the instructions 151 refer to identical locations in external memory.*
>
> For example, suppose that a first instruction 151 to store data refers to a location in external memory determined as (contents of register A) + (fixed offset value B), and a second instruction 151 to load data refers to the same location in external memory determined as (contents of register A) + (fixed offset value B), where A and B are identical. In this case, the microprocessor 100 can proceed with the knowledge that the first (store) instruction 151 and the second (load instruction) 151 refer to the same location. Since the second (load) instruction 151 is going to read the same data from external memory that the first (store) instruction 151 put there, the microprocessor 100 can proceed by using that data from an internal register, rather than waiting for external memory to complete actual store and load operations.

Specification, page 8, line 20 to page 9, line 22 (emphasis added). Accordingly, the specification as filed describes the subject matter of the limitations on which the rejection is based.

Therefore, the rejection of claims 2-3, 6-13 and 16-19 under 35 U.S.C. § 112, first paragraph has been overcome.

35 U.S.C. § 112, Second Paragraph (Definiteness)

Claims 2-3, 6-13 and 16-19 were rejected under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter that the applicant regards as the invention. This rejection is respectfully traversed.

The Office Action states:

> As per claims 2 and 12, taking claim 2 as exemplary, the claim recites "***detecting*** *a first instruction* ***using first base and offset address values*** *to load data from a first memory location that was previously stored to, wherein the first instruction is* ***detected based upon the first base and offset address*** *values and* ***without*** *using a memory address corresponding to* ***the first base and offset address values***." The claim appears to be vague and indefinite. The claim appears to contradict itself, it detects the first instruction using the base and offset address value and later in the claim the detection is based on the based and offset value but without using the address corresponding to the first base and offset address value. Thus, it is not clear how it is detecting based on the base and offset address values but not using them.

Paper No. 20090113, pages 3-4 (emphasis in original). As noted above, the specification teaches detecting instructions accessing a memory location X corresponding to base value A plus offset value B using the base and offset values A, B and without computing X = A + B. The claim limitations are not contradictory.

Therefore, the rejection of claims 2-3, 6-13 and 16-19 under 35 U.S.C. § 112, second paragraph has been overcome.

35 U.S.C. § 102 (Anticipation)

Claims 2, 12 and 20 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,216,200 to *Yeager*. Claims 2-3, 6-13 and 16-21 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,666,506 to *Hesson et al.* These rejections are

respectfully traversed.

A claim is anticipated only if each and every element is found, either expressly or inherently described, in a single prior art reference. The identical invention must be shown in as complete detail as is contained in the claim. MPEP § 2131 at p. 2100-67 (8th ed. rev. 6 September 2007).

Independent claims 2 and 12 each recite detecting a first instruction using first base and offset address values to load data from a first memory location that was previously stored to, wherein the first instruction is detected based upon the first base and offset address values and without using a memory address equaling to the first base address value added to the offset address value. Such a feature is not found in the cited references. *Yeager* teaches comparing virtual addresses that are, for indexed address calculations, formed by "base+index." *Yeager*, column 9, lines 21-22. *Hesson et al* does not, as asserted in the Office Action, teach that the virtual addresses employed have base and effective addresses.

Claim 20 recites using the syntax for the first instruction and the syntax for the second instruction to determine a relationship between the first memory location and the second memory location, without using the effective address for the first memory location or the effective address for the second memory location. Such a feature is not found in the cited references. Both *Yeager* and *Hesson et al* teach using the virtual addresses – that is, the effective addresses, as opposed to the physical or "real" addresses – of memory locations to determine correspondence of two memory locations. The interpretation of "using the effective address for the first memory location" as being limited to "using the effective address to access the memory location is arbitrary and capricious. No basis for such as limitation, other than to contrive a basis for rejection of the claim, exists.

Therefore, the rejection of claims 2-3, 6-13 and 17-21 under 35 U.S.C. § 102 has been overcome.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***dvenglarik@munckcarter.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication (including any extension of time fees) or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

MUNCK CARTER, LLP

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Daniel E. Venglarik
Registration No. 39,409

Docket Clerk
P.O. Box 802432
Dallas, Texas 75380
Phone: (972) 628-3600
Fax: (972) 628-3616
E-mail: *dvenglarik@munckcarter.com*